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(71) Applicant: ULTRATECH STEPPER INC. [US/US]; 3050 Zanker Road, San Jose, CA 95135 (US).

(72) Inventors: TALWAR, Somit; 3348 Vernon Terrace, Palo Alto, CA 94303 (US). KRAMER, Karl-Josef; Apartment 17, 810 Coleman Avenue, Menlo Park, CA 94025 (US). VERMA, Guarav; 3348 Vernon Terrace, Palo Alto, CA 94303 (US). WEINER, Kurt; 822 Nevada Avenue, San Jose, CA 95125 (US).

(74) Agents: JONES, Allston, L. et al.; Peters, Verny, Jones & Bikša, L.L.P., Suite 6, 385 Sherman Avenue, Palo Alto, CA 94306-1840 (US).

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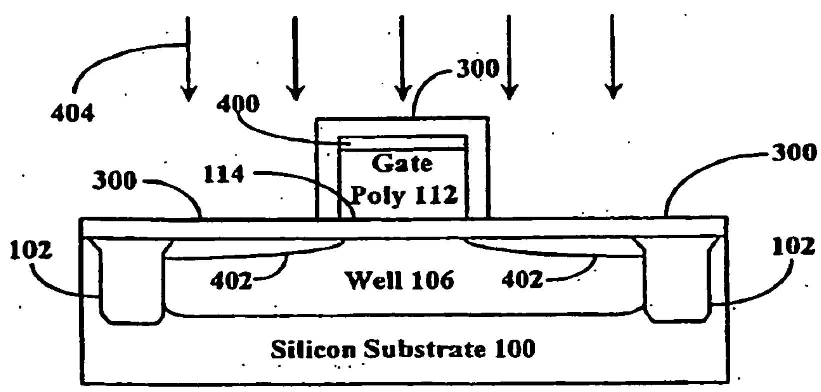

(57) Abstract

Pre-amorphization of a surface layer of crystalline silicon to an ultra-shallow (400) and (402) (e.g., less than 100 nm) depth provides a solution to fabrication problems including (a) high thermal conduction in crystalline silicon and (b) shadowing and diffraction-interference effects by an already fabricated gate of a field-effect transistor on incident laser radiation. Such problems, in the past, have prevented prior-art projection gas immersion laser doping from being effectively employed in the fabrication of integrated circuits comprising MOS field-effect transistors employing 100 nm and shallower junction technology.

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INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :HO1L 21/8238
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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/199, 486, 487, 482, 483, 508, 530, 542, 557, 575, For. 154, For. 319, For. 334, For. 408; 148/DIG. 61

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,147,826 A (LIU et al.) 15 SEPTEMBER 1992 (15.09.92), col. 3, line 25 to col. 6, line 30.	1-17
A	US 5,342,793 A (SANTAGELO et al.) 30 AUGUST 1994 (30.08.94), col. 1, line 65 to col. 4, line 50.	1-17
A	US 5,407,838 A (OHMISHI et al.) 18 APRIL 1995 (18.04.95), col. 1, line 65 to col. 5, line 5.	1-17
A	US 4,617,066 A (VASUDEV) 14 OCTOBEBER 1986 (14.10.86), col. 2, line 55 to col. 12, line 5.	1-17

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
19 AUGUST 1998	06 NOV 1998

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4,904,611 A (CHIANG et al.) 27 FEBRUARY 1990 (27.02.90), col. 2, line 55 to col. 7, line 35.	1-17
A	US 5,470,619 A (AHN et al.) 28 NOVEMBER 1995 (28.11.95), col. 2, line 40 to col. 6, line 25.	1-17
A	US 5,470,619 A (AHN et al.) 28 NOVEMBER 1995 (28.11.95), col. 2, line 40 to col. 6, line 25.	1-17

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Pre-amorphization of a surface layer of crystalline silicon to an ultra-shallow (e.g., less than 100 nm) depth provides a solution to fabrication problems including: (1) high thermal conduction in crystalline silicon and (2) shadowing and diffraction-interference effects by an already fabricated gate of a field-effect transistor on incident laser radiation. Such problems, in the past, have prevented prior-art projection gas immersion laser doping from being effectively employed in the fabrication of integrated circuits comprising MOS field-effect transistors employing 100 nm and shallower junction technology.

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FABRICATION METHOD FOR REDUCED-DIMENSION INTEGRATED CIRCUITS

BACKGROUND OF THE INVENTION

Field of the Invention:

This invention relates to the fabrication of integrated circuits (IC) and, more particularly, to the fabrication of IC comprising metal oxide semiconductor field-effect transistors (MOSFET) employing 100 nm and shallower junctions.

Description of the Prior Art:

CMOS field-effect transistors (FET) employing 0.25 mm gate length dimensions will soon be commercially available. Fabrication of such 0.25 mm dimension FETs typically employs ion implantation for silicon doping. However, MOSFETs having reduced gate-length dimensions of only 0.18 mm and lower are currently being developed. Reduction of gate lengths necessitates source-drain junction depth scaling. For the 0.18 mm CMOS technology, these junctions depths are projected, by the Semiconductor Industry Association's "The National Technical Roadmap for Semiconductors" (1995), to be at less than 80 nm Such junctions are difficult to form using ion implantation due to ion-channeling and transient enhanced diffusion.

Incorporated by reference herein is in the article "Two-Step Doping Using Excimer Laser in Boron Doping of Silicon," by T. Akane et al., Jpn. J. Appl. Phys. Vol. 31 (Dec. 1992) Pt. 1, No. 12B, pages 4437-4440, which discloses an alternative means for silicon doping. In this regard, further incorporated by reference herein is the article "A Shallow Junction Submicrometer PMOS Process Without High-Temperature Anneals," by P. G. Carey et al., IEEE Electron Device Letters, Vol. 9, No. 10, (Oct. 1988), pages 542-544.

Also incorporated by reference herein are the articles "Role of Ion Mass, Implant Dose, and Wafer

Temperature on End-of-Range Defects," by S. Prussin et al., J. ElectroChem. Soc., Vol. 137, No. 6 (June. 1990), pages 1912-1914; "Damage Removal/Dopant Diffusion Tradeoffs in Ultra-Shallow Implanted p^+-n Junctions," by R. B. Fair, IEEE Transactions on Electron Devices, Vol. 17, No. 10 (Oct. 1990), pages 2237-2241, and "Avoiding End-of-Range Dislocations in Ion-Implanted Silicon," by S. Acco et al., Materials Science and Engineering, B34, (1995) pages 168-174, all of which are directed to ion implantation to effect silicon amorphization.

Were it not for the high thermal conduction in crystalline silicon, ultra-shallow (e.g., less than 100 nm) junction formation would be possible using prior-art projection gas immersion laser doping (P-GILD), due to near surface absorption of the laser light and short laser pulse widths. In this regard, the geometry of an MOSFET device being fabricated results in shadowing and diffraction of the laser light illuminating the device's surface which has a large effect on thermal loading. Unfortunately, the high thermal conduction in crystalline silicon acts to reduce the junction depth at the edges. These thermal conduction effects become apparent as the dimensions of the doped regions approach the thermal diffusion lengths. As a result, the attributes of the doped region are a function of their dimensions and the surrounding geometry. In the case of source/drain doping in a CMOS device, this results in the doped regions not extending up to the gate (negative gate overlap) or the isolation. This presents an unacceptable problem, since device performance suffers due to high parasitic resistances and shorts between the junctions and the wells.

SUMMARY OF THE INVENTION

The fabrication method of the present invention provides a solution to the aforesaid problem of thermal diffusion, thereby permitting P-GILD to be used for achieving ultra-shallow (e.g., less than 80 nm) junction

formation.

More particularly, in accordance with the fabrication method of the present invention, a given surface layer of crystalline silicon is first amorphized to a given depth. Thereafter a given amount of doping material is deposited as a film on the surface of the given amorphized surface layer of the silicon. Then at least a portion of the given amorphized surface layer of the silicon is temporarily heated for a certain time to a temperature which is sufficient to melt amorphized silicon but is insufficient to melt crystalline silicon (since the melting temperature of amorphized silicon is substantially below that of crystalline silicon). After the completion of the certain heating time, the melted silicon of the heated portion is permitted to cool, thereby effecting a recrystallization of the silicon of this portion of the given surface layer.

BRIEF DESCRIPTION OF THE DRAWING

FIGURE 1 diagrammatically shows the structure of two FETs that have been fabricated in accordance with modern silicon CMOS technology;

FIGURE 2a diagrammatically shows the pattern of heat diffusion from the heated upper region of an MOSFET that occurs when P-GILD is used in its fabrication;

FIGURE 2b diagrammatically shows the shadowing and diffraction-interference effects caused by the gate polycrystalline (poly) structure of an MOSFET that occurs when P-GILD is used in its fabrication;

FIGURE 3 diagrammatically shows the structure of one of the two FIGURE 1 MOSFETs that is to be fabricated in accordance with the method steps of the present invention at a stage in the fabrication of that FET which occurs prior to either the doping of its extensions or the doping of its source or drain, but subsequent to the doping of its well;

FIGURE 4 diagrammatically shows a fabrication step of the present invention comprising surface

amorphizing by ion implantating the silicon forming the upper region of the MOSFET of FIGURE 3; and

FIGURE 5 diagrammatically shows a fabrication doping step of the present invention (which occurs subsequent to both the FIGURE 4 fabrication step of surface amorphization and other intervening fabrication steps that include radiation from a first laser operation having been used to photolytically predeposit a film of doping material) which uses the radiation from a second laser to effect a doping which includes both the extensions and the gate poly of that FET with the predeposited film of doping material.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIGURE 1, there is shown CMOS structure comprising silicon substrate 100, isolation elements 102 and complimentary FETs 104a and 104b. The structure of complimentary FETs 104a and 104b differ only in that FET 104a comprises n well 106a, p^+ source 108a and p^+ drain 110a, while FET 104b comprises p well 106b, n^+ source 108b and n^+ drain 110b. In all other respects, the structure of complimentary FETs 104a and 104b is similar. Specifically, both of complimentary FETs 104a and 104b comprise (1) gate poly 112 insulated from the well of that FET by a thin layer 114 of SiO_2, (2) side wall spacers 116, (3) silicide electrical contacts 117 situated on top of the respective gate poly, source and drain of each of complimentary FETs 104a and 104b, and (4) shallow doped extensions 118 coupling the source and drain of each of complimentary FETs 104a and 104b to the channel region under the gate poly.

It is apparent from FIGURE 1 that the shallowest junctions are extensions 118, which connect the deep sources and drains to the channel. Extensions 118 are needed to prevent drain induced barrier lowering (DIBL) and punchthrough. The extensions are currently formed by a shallow low energy implant and anneal, after which side wall spacers are formed and deep source/drains

implanted.

At this time, the smallest gate dimensions soon to be employed in the commercial fabrication of MOSFET structures is 0.25 mm In this case, extensions 118 are currently formed by a relatively shallow low energy implant and, thereafter, the p^+ and n^+ sources 108a and 108b and drains 110a and 110b are formed by a relatively deep high energy ion implant. However, when the fabrication of MOSFET structures is scaled down to 0.18 mm gate lengths, the already shallow junction depth of extensions 118 is reduced to less than 80 nm. Such a small junction depth for extensions 118 is difficult to form using ion implantation due to ion-channeling and transient enhanced diffusion.

As discussed above in the Background of the Invention section, problems that result from the high thermal conduction in crystalline silicon have prevented the prior-art P-GILD doping technique from being used in place of ion implantation to form less than a 80 nm deep junction for each of extensions 118.

FIGURE 2a demonstrates only the heat diffusion pattern in that portion of the silicon of the MOSFET being fabricated that is relatively nearer to gate 202 than to the IC isolation elements. Prior-art P-GILD, if used during the fabrication of an IC MOSFET device, would heat the entire single crystalline silicon upper surface layer 200 between adjacent IC isolation elements. Far from gate 202, the heating can be modeled using one-dimensional heat diffusion (as indicated in FIGURE 2 by solid-line arrows 204). However, the region under gate 202, which is shadowed from the laser light, remains cooler than regions far from gate 202. Hence, in the vicinity of gate 202, both vertical and lateral, thermal gradient exists. This results in 2-D thermal diffusion in the vicinity of gate 202 (as indicated in FIGURE 2a by dashed-line arrows 206). Therefore, cooling is enhanced in this vicinity, leading to shallower or no melting,

should prior-art P-GILD laser radiation be employed in the fabrication of the FET.

Further, although not shown in FIGURE 2a, it is apparent that a two-dimensional heat diffusion pattern would also exist during the fabrication of each of the CMOS FETs of FIGURE 1 at the junction of that FET's source and drain regions with an isolation element, if prior-art P-GILD laser radiation were employed in its fabrication.

FIGURE 2b schematically depicts both the shadowing effect 208 and the diffraction-interference effect 210 caused by the presence of the gate 202. More particularly, within the area of the top silicon surface defined by each oblique dashed line 212 and a vertical sidewall of gate 202, the shadowing effect is schematically indicated by boxes 214 and the diffraction-interference effect is schematically indicated by boxes 216.

FIGURE 2b demonstrates illumination effects near the gate edge. Due to the large numerical aperture of a P-GILD projection system, the angle of incidence varies from 90 to 50 degrees. As a result of angular spread of the illuminating laser light, shadowing by the gate can reduce up to 50% of the light in the region next to it. Some of the fluence loss may be compensated for by additional light reflected off of the silicon sidewall of gate 202. However, it can be shown that silicon exhibits low reflectivity of TM polarized light at near grazing angles. It can be seen that due to this low reflectivity of TM polarized light, a large amount of the light incident on the gate sidewall is in fact absorbed. Hence, reflection off gate 202 cannot completely compensate for the fluence loss due to shadowing. Further, diffraction from the edge of gate 202 and interference between the reflection off of gate 202 and the incident light reduces the incident intensity next to the edge of gate 202. This results in the near gate

region being colder than the rest of the source and drain regions.

Thus, the combination of enhanced cooling and shadowing at the gate edge can prevent the melt from extending up to the edge of gate 202. Although it is possible for the melt to reach gate 202 at sufficiently high laser energies, the use of such high laser energies is undesirable. Further, the negative overlap between gate 202 and the melt increases with increasing gate length due to larger thermal gradients under gate 202. A modern circuit may be comprised of devices with varying gate lengths. As a result, the negative overlap will vary for the different devices. A negative overlap results in high series resistances and large leakage to the substrate. Such junctions are unacceptable for modern CMOS technology and methods for ensuring that junctions extend to the gate for all gate lengths needs to be devised.

In addition, two-dimensional cooling can also prevent melting near the edge of an isolation element, thereby causing a short to be created between the junction and the well when silicidation is performed. As a result, the drain cannot be biased with respect to the well. Hence, melting up to the isolation element 102 is extremely important.

The relatively simple process performed by the method of the present invention, shown in FIGURES 3-6 and described below, avoids the aforesaid problems of negative overlay due to two-dimensional cooling and reduction in laser fluence due to shadowing and diffraction-interference, which problems are encountered when prior-art P-GILD laser radiation is employed in the fabrication of the MOSFETs of FIGURE 1.

FIGURE 3 shows a stage in the fabrication of one of the MOSFETs of FIGURE 1 just prior to the execution of fabrication steps which include the fabrication steps of the present invention shown in

FIGURES 4 and 5. At the fabrication stage shown in FIGURE 3, well 106, and gate poly 112 situated over a thin layer 114 of SiO_2 have already been fabricated.

The first of the fabrication steps of the present invention, shown in FIGURE 4, comprises the step of amorphizing, to a desired ultra-shallow depth, regions of the FIGURE 1 MOSFET being fabricated which include the upper polycrystalline silicon layer 400 of gate poly 112 and the upper single silicon crystalline layers 402 of well 106. Amorphization may be achieved by ion implantation of a heavy atom, such as argon, silicon, and germanium (as indicated in FIGURE 4 by arrows 404). However, germanium is to be preferred because it is a heavy atom which requires low doses to amorphize silicon, produces abrupt amorphous-crystalline interfaces, and is isoelectronic in the silicon lattice.

More particularly, as shown in FIGURE 4, layer 402 on each side of gate poly 112, which is to be amorphized, extends all the way to an isolation element 102. Assuming, by way of example, that the desired ultra-shallow depth of the layers 400 and 402 to be amorphized is substantially 300 Å (which is less than 80 nm), a dose of 2×10^{14} atoms/cm^2 is required to achieve this desired 300 Å amorphization depth. A 20 KeV germanium implant at a dose of 2×10^{14} atoms/cm^2 achieves this desired 300 Å amorphization depth of the layers 400 and 402. This implant condition is easily obtainable using existing implanters.

As is known (see the aforesaid R. B. Fair article incorporated by reference), the amorphous depth is a function of implant dose and implant energy. Depending on the desired amorphous depth, the range of implant dose is between 1×10^{13} atoms/cm^2 and 1×10^{16} atoms/cm^2, while the range of implant energy is between 5 KeV atoms/cm^2 and 400 KeV.

Subsequent to the completion of the silicon amorphization fabrication step of FIGURE 4, two

fabrication steps (neither of which is shown in the drawing) take place which comprise (1) the removal of thin layer 300 of SiO_2, followed by (2) the first step of a known P-GILD operation (e. g., that disclosed above in the article "Two-Step Doping Using Excimer Laser in Boron Doping of Silicon," by T. Akane et al.) which uses an ArF excimer laser (l = 193 nm) to decompose, presumably by photolytic decomposition, a given dopant compound in gaseous form to thereby cause a film of doping material in solid form to be predeposited on the upper surfaces of the MOSFET being fabricated. The amount of the dose to be incorporated in amorphized layers 400 and 402 during the second step of the known P-GILD operation depends on the amount of the given dopant compound that has been predeposited during the first step of the known P-GILD operation.

Referring to FIGURE 5, there is shown the second step of the P-GILD operation, which takes place at the completion of the aforesaid two unshown fabrication steps. As shown in FIGURE 5, predeposited film 500 of doping material on the upper surfaces of layers 400 and 402 of the MOSFET being fabricated is illuminated by excimer laser radiation 502. While this excimer laser radiation may be derived from an ArF excimer laser producing radiation at a wavelength of 193 nm (as taught in the T. Akane et al. article)., it also may be derived from other types of lasers (e.g., a 248 nm KrF laser, a 351 nm XeF laser, or a 308 nm XeCl laser). Applicant has employed a pulsed XeCl excimer laser producing radiation at a wavelength of 308 nm for performing the aforesaid second step of the P-GILD operation.

More particularly, amorphous silicon has a factor of 10 lower thermal conductivity, a 300 °C lower melt temperature, and a 30 percent lower reflectivity than crystalline silicon. The combination of these effects lowers the melt threshold of amorphous silicon compared to crystalline silicon.

Referring again to FIGURE 1, in the process for forming extensions 118, the depth of the amorphized layers is limited to that needed for the regions to be occupied by each of these extensions. Thereafter, the second step of the P-GILD operation, used in lightly doping the regions of extensions 118, results in the amorphized layers of silicon melting right up to the edge of gate poly 112, due to the significant reduction in the thermal conductivity and melt temperature of these amorphized layers. More specifically, the second step of the P-GILD operation comprises each of successive pulses of laser radiation. The irradiating energy of each of the successive pulses is sufficient to cause melting of an amorphized silicon spot, but is insufficient to cause melting of a crystalline silicon spot. After the completion of the first irradiation of a particular spot by a laser pulse, the now-doped melted silicon thereof immediately cools and recrystallizes. Therefore, the irradiation by a first pulse of a given amorphized silicon spot that overlaps the recrystallized silicon of an already irradiated spot will not cause any remelting of the recrystallized silicon, but will result only in the melting of the given amorphized silicon spot. Further, a large energy window exists where melting will not extend beyond the amorphous regions, since the liquid silicon is highly undercooled and cannot produce further silicon melting. Hence, amorphization can be used to define the melt depth.

While the fluence range for laser irradiation extends all the way from 0.05 Joules per cm^2 and 1.0 Joules per cm^2, the most likely radiation fluence sufficient to heat amorphized silicon to its melting temperature, but insufficient to heat crystalline silicon to its melting temperature, is 0.4 Joules per cm^2.

As indicated in FIGURES 4 and 5, layer 400 of gate poly 112 is both amorphized and doped. In the case that doping of gate poly 112 is not desired, a masking

layer over gate poly 112 may be employed during the amorphization implanting step of FIGURE 4, thereby preventing gate melting of gate poly 112 to take place during the second step of the P-GILD operation.

While the use of two steps of P-GILD following silicon preamphorization is particularly suitable for fabricating the ultra-shallow (i.e., less than 100 nm depth) junctions of extensions 118, as described above, the same two steps of P-GILD following silicon preamphorization may be used to dope the deep source and drain regions of a MOSFET being fabricated. Specifically, following the fabrication of the ultra-shallow junctions of extensions 118, side wall spacers 116 are fabricated. Thereafter, each the deep source and drain regions located between each side wall spacer 116 and an isolation element 102 is reamorphized to its greater desired depth than the depth of the above-described original amorphization thereof. This may be accomplished with higher energy (e.g., 40 KeV) and higher dose (e.g., 6×10^{14} atoms/cm^2 germanium implants). Following such reamorphization, the two steps of P-GILD are used to provide (1) appropriate deposited concentrations of films of doping material during the first of these two steps, and (2) appropriate pulsed laser energy to effect melting of only the amorphised source and drain regions during the second of these two steps.

One reason for employing the steps of the present invention described in the preceding paragraph for doping the deep source and drain, rather than conventional ion-implant doping, is that the doping depth is more precisely controlled. An additional reason is that it is less expensive.

In the method of the preferred embodiment of the present invention described above, the fabrication of the deep source and drain involve the reamorphization of the already-fabricated ultra-shallow (i.e., less than 100

nm depth) junctions, since these already-fabricated ultra-shallow junctions extend all the way to side wall spacers 116. However, it should be understood that the extent of the ultra-shallow junctions may be limited to solely the locations of the extensions and, therefore, not include the locations of the deep source and drain. In this case, the amorphization for the source and drain locations is independent of the amorphization for the extension locations, so that the amorphization for the source and drain locations may occur either before or after the amorphization for the extension locations. Furthermore, the present invention may be employed for fabricating only the extensions of an MOSFET or, alternatively, only the deep source and drain of an MOSFET, rather than both of these.

As known, amorphization implants produce supersaturation of point defects. Upon annealing, point defect injection results in nucleation of extended defects. A critical annealing temperature ordinarily is required to anneal out the extended defects. This ordinarily required anneal for the first amorphization implant, shown in FIGURE 4 and described above, is at 1050 °C for 10 sec. However, the laser melting of the amorphized silicon by the second step of the P-GILD operation inherently provides a certain amount of annealing. Further, due to the small number of point defects present after the laser process, the junctions are not likely to move much as a result of this thermal cycle. Therefore, in this case, no additional anneal for laser annealed junctions may be necessary. However, in any given case, the exact extent of the diffusion after laser annealing needs to be determined experimentally in order to determine if any additional annealing is necessary.

WHAT IS CLAIMED IS:

1. In a method for fabricating source drain junctions of an MOSFET on a substrate comprising a given crystalline silicon surface layer, wherein said method comprises the steps of:

(a) amorphizing silicon of said given crystalline silicon surface layer of said substrate to a given amorphization depth;

(b) thereafter depositing a given amount of doping material as a film on the surface of said given amorphized silicon surface layer; and

(c) then temporarily heating at least a portion of said given amorphized surface layer of said silicon for a certain time to a temperature which is sufficient to melt amorphized silicon but is insufficient to melt crystalline silicon to thereby result in said deposited dopant diffusing into said given melted amorphized silicon surface layer;

whereby the melted silicon of said portion cools after said certain time to thereby effect a recrystallization of the silicon of said portion of said given surface layer.

2. The method defined in Claim 1, wherein said given amorphized depth of silicon overlies crystalline silicon.

3. The method defined in Claim 1, wherein step (a) comprises the step of:

(d) amorphizing said given surface layer of said silicon to a given amorphization depth by implanting therein atoms of a given heavy element at a given concentration per unit area that have been ionized and accelerated to a given energy by an ion implanter.

4. The method defined in Claim 3, wherein said given heavy element is germanium.

5. The method defined in Claim 3, wherein said given concentration per unit area is substantially 2

x 10^{14} atoms/cm^2 and said given energy is substantially 20 KeV.

6. The method defined in Claim 3, wherein said given concentration per unit area is substantially 6 x 10^{14} atoms/cm^2 and said given energy is substantially 40 KeV.

7. The method defined in Claim 1, wherein step (b) comprises the step of:

(d) employing radiation from of a laser to decompose a given dopant compound in gaseous form to thereby cause said given amount of doping material to be deposited in solid form as said film on the surface of said given amorphized silicon surface layer.

8. The method defined in Claim 1, wherein step (c) comprises the step of:

(d) employing a given amount of radiant fluence from a laser to effect said temporary heating of at least said portion of said given amorphized surface layer of said silicon.

9. The method defined in Claim 8, wherein said given amount of radiant fluence from said laser is substantially 0. 4 Joules per cm^2.

10. The method defined in Claim 8, wherein step (d) comprises the step of:

(e) applying a single one of successive pulses of radiant energy from a pulsed laser to an irradiated area of said given amorphized surface layer of said silicon for heating said area for the duration of that single one of said successive pulses, the radiation energy of that single one of said successive pulses being sufficient to heat the amorphized silicon of said area irradiated thereby to its melting temperature, but insufficient to heat crystalline silicon to its melting temperature.

11. In an integrated circuit fabrication method for fabricating MOSFETs on a silicon substrate, wherein adjacent FETs are separated from one another by

isolation elements and each fabricated FET comprises (1) a polycrystalline silicon gate built up over (2) the surface of an appropriately-doped single crystalline silicon well, (3) first and second sidewall spacers situated, respectively, on either side of said polycrystalline silicon gate (4) a relatively deep appropriately-doped single crystalline silicon source extending longitudinally from a first isolation element to the vicinity of the distal edge of said first sidewall spacer, (5) a relatively deep appropriately-doped single crystalline silicon drain extending longitudinally from a second isolation element to the vicinity of the distal edge of said second sidewall spacer, (6) a first ultra-shallow, lightly-doped single crystalline silicon extension situated under said first sidewall spacer for connecting said source to a gate edge proximate thereto, and (6) a second ultra-shallow, lightly-doped single crystalline silicon extension situated under said second sidewall spacer for connecting said drain to a gate edge proximate thereto; wherein said method comprises the following steps for fabricating each of said first and second ultra-shallow, doped single crystalline silicon extensions subsequent to the fabrication of said well and said polycrystalline silicon gate and prior to the fabrication of said first and second sidewall spacers:

(a) ion implanting atoms in each of first and second surface layers of said single crystalline silicon well that extend longitudinally from a gate edge of said polycrystalline silicon gate to an isolation element at a given concentration per unit area and at a given energy which results in amorphizing said first and second layers to a certain depth which is less than 100 nm deep;

(b) depositing a given amount of doping material for doping said extensions as a film in solid form on said first and second amorphized surface layers by decomposing a given dopant compound in gaseous form with radiation from of a laser;

(c) first applying a first of two successive pulses of radiant energy from a pulsed laser to a first of two overlapping irradiated areas of said given amorphized surface layer of said silicon for heating said first area for the duration of said first of said successive pulses, and thereafter applying a second of said two successive pulses of radiant energy from said pulsed laser to a second of said two overlapping irradiated areas of said given amorphized surface layer of said silicon for heating said second area for the duration of said second of said successive pulses, the radiation energy of each separate one of said first and second successive pulses being sufficient to heat the amorphized silicon of said area irradiated thereby to its melting temperature, but insufficient to heat crystalline silicon to its melting temperature; and

(d) providing a time interval between the application of said first of said two successive pulses and the application of said second of said two successive pulses that is long enough to permit the melted amorphized silicon of said first of said two overlapping areas to cool and recrystallize prior to the application of said second of said two successive pulses to the amorphized silicon of said second of said two overlapping areas.

12. The method defined in Claim 11, wherein said given concentration per unit area of said ion-implanted atoms is substantially 2×10^{14} atoms/cm^2 and said given energy is substantially 20 KeV.

13. The method defined in Claim 11, wherein said ion implanted atoms are germanium.

14. The method defined in Claim 12, wherein:

said given concentration per unit area of said ion-implanted germanium atoms is substantially 2×10^{14} atoms/cm^2 and said given energy is substantially 20 KeV;

whereby the amorphized depth of said first and second layers is substantially 300 Å.

15. The method defined in Claim 11, further wherein step (a) further comprises ion implanting germanium atoms in an upper surface layer of said polycrystalline silicon gate at a given concentration per unit area and at a given energy which results in amorphizing said upper surface layer of said polycrystalline silicon gate to a certain depth which is about 300 Å deep.

16. The method defined in Claim 11, further comprising the following steps for fabricating each of said relatively deep appropriately-doped single crystalline silicon source and drain subsequent to the fabrication of said first and second sidewall spacers:

(a) ion implanting atoms at a concentration of substantially 6×10^{14} atoms/cm^2 and at an energy of 40 KeV in each of (1) a source layer of said single crystalline silicon that extends longitudinally from an edge of said first sidewall spacer to an isolation element and (2) a drain layer of said single crystalline silicon that extends longitudinally from an edge of said second sidewall spacer to an isolation element, which results in amorphizing said source and drain layers to the relatively deep depth required for said source and drain;

(b) depositing a given amount of doping material for appropriately doping said source and drain layers as a film in solid form on the surface of said amorphized source and drain layers by photolytically decomposing a given dopant compound in gaseous form with radiation from of a laser;

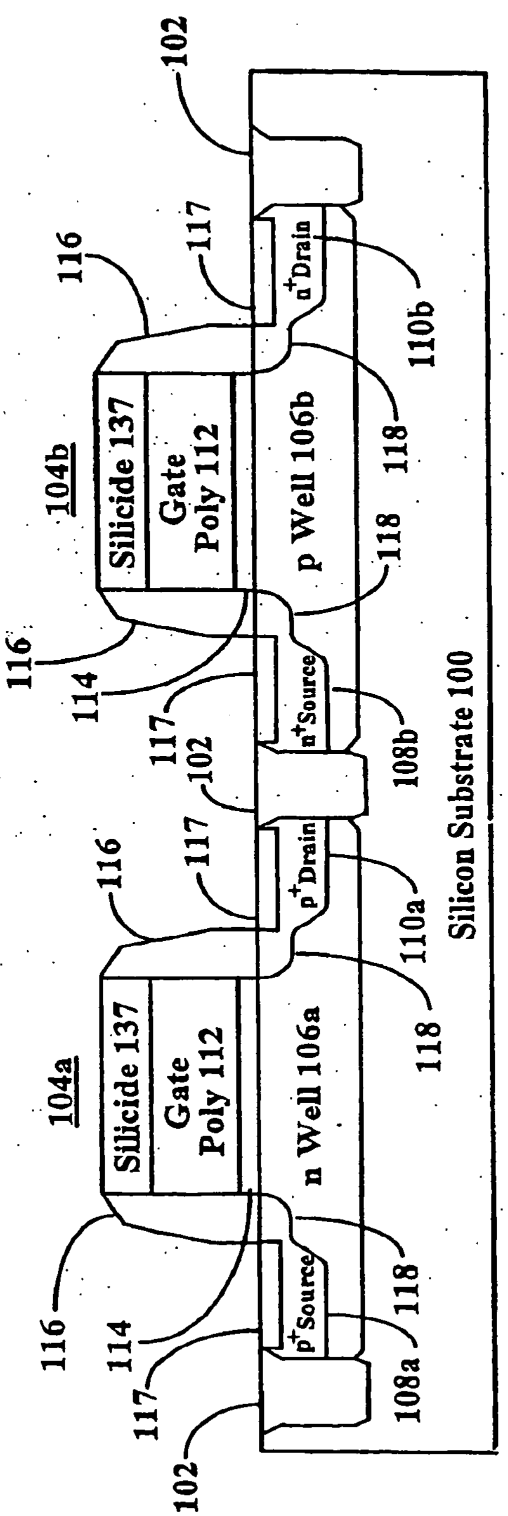
(c) first applying a first of two successive pulses of radiant energy from a pulsed laser to a first irradiated area of a certain one of said source and drain amorphized layers of said silicon for heating said first area for the duration of said first of said successive pulses, and thereafter applying a second of said two successive pulses of radiant energy from said pulsed

laser to a second irradiated area of said certain one of said source and drain amorphized layers of said silicon that at least partially overlaps said first irradiated area for heating said second area for the duration of said second of said successive pulses, the radiation energy of each separate one of said first and second successive pulses being sufficient to heat the amorphized silicon of said area irradiated thereby to its melting temperature, but insufficient to heat crystalline silicon to its melting temperature; and

(d) providing a time interval between the application of said first of said two successive pulses and the application of said second of said two successive pulses that is long enough to permit the melted amorphized silicon of said first area to cool and recrystallize prior to the application of said second of said two successive pulses to the amorphized silicon of said second area.

17. The method defined in Claim 16, further comprising:

(e) repeating steps (c) and (d) for the other of said source and drain amorphized layers of said silicon from said certain one thereof.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102
117
p+Drain
110a
116
118
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116
114
p+Source
117
108a
102

Fig. 1

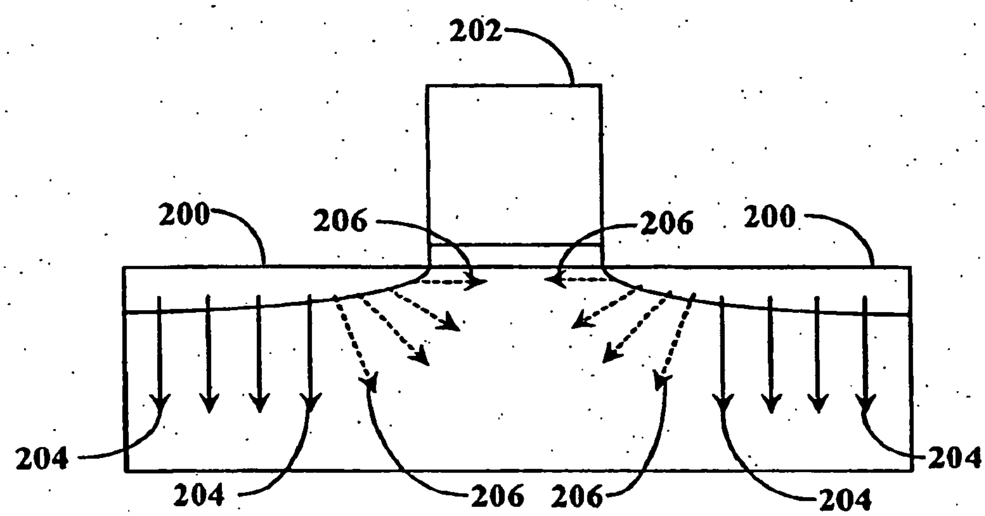
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Fig. 2A

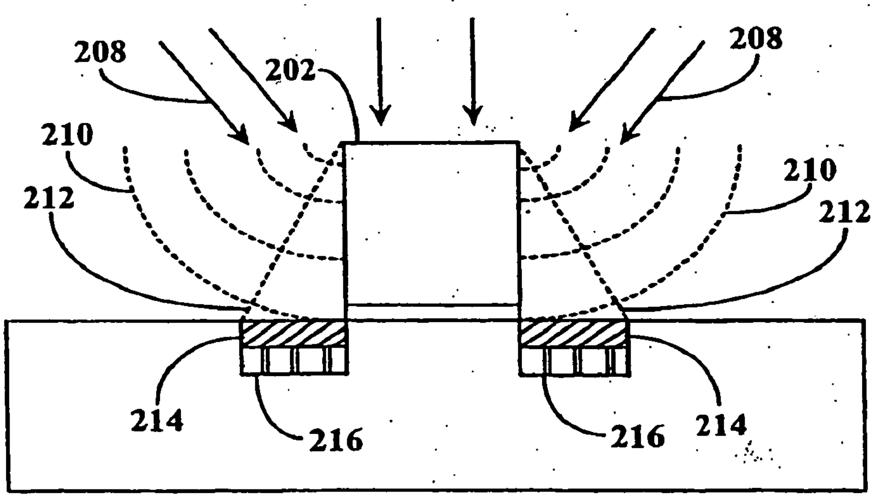
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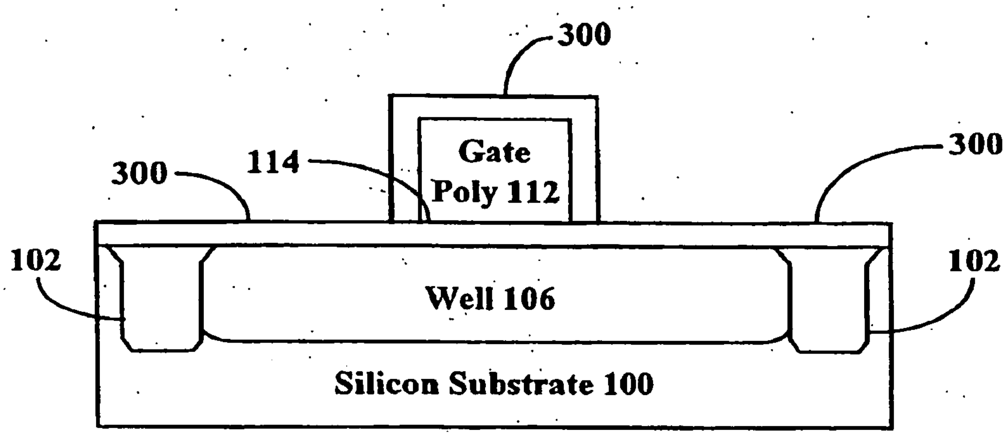
Fig. 2B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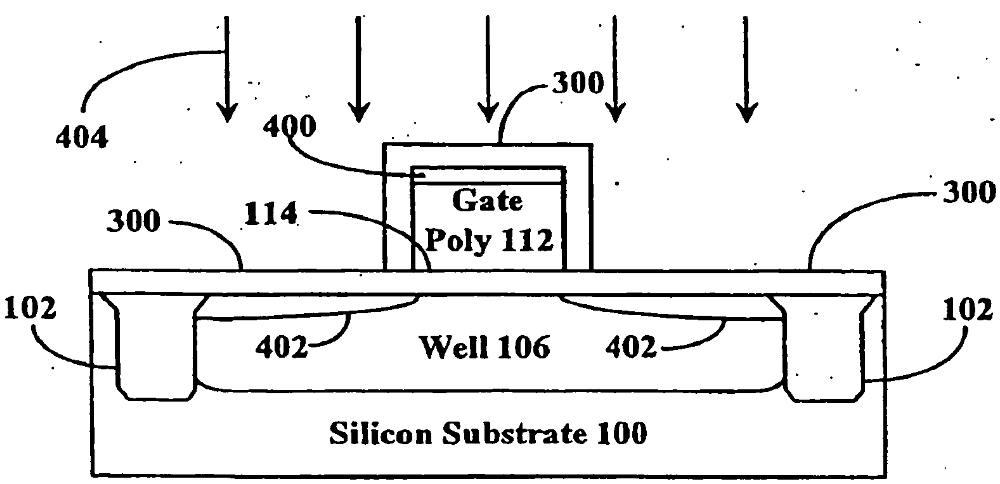
300
114
300
102
Well 106
102
Silicon Substrate 100

Fig. 3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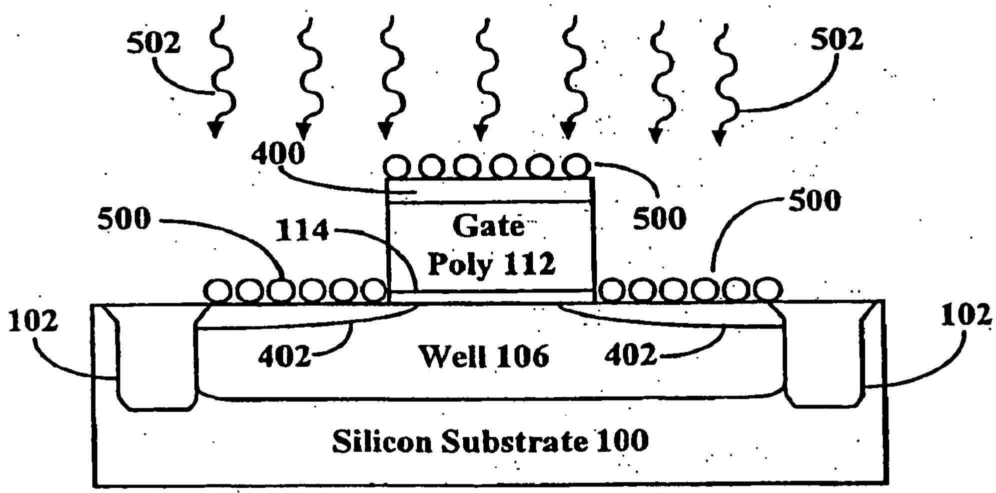
300
102
402
Well 106
402
102
Silicon Substrate 100

Fig. 4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500
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114
Gate
Poly 112
102
102
402
Well 106
402
Silicon Substrate 100

Fig. 5